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13. ABSTRACT *(Maximum 200 words)*

The primary objective of this Phase I project was to determine the extent of the significant reduction in power consumption of integrated circuits which may be achieved by utilizing a novel sidegate FET technology. The new FET technology eliminates the Narrow Channel Effect (NCE) which is one of the primary factors limiting the minimum power consumption of integrated circuits. By eliminating the NCE, we may scale the device size dramatically and reduce the power-delay product by at least an order of magnitude compared to existing transistor technologies. Additionally, the new FET has two gates which can therefore lead to a significant reduction in the transistor count of ICs, as was demonstrated in a simple NOR gate using only two transistors. Finally, the transistor technology is compatible with HFET circuits for microwave/digital applications. In this Phase I project, the design, fabrication, characterization and modeling of the new transistor was investigated and issues concerning manufacturability were discussed.

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Novel Field Effect Transistors for Low Power Electronics

Final Report

NAVY STTR Phase I
Contract Number: N00014-94-C-0260

May 15, 1995

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Novel Field Effect Transistors for Low Power Electronics
(ONR STTR Contract N00014-94-C-0260)

Table of Contents

I. Phase I Technical Objectives

The primary objective of this Phase I project is to determine the extent of the significant reduction in power consumption of integrated circuits which may be achieved by utilizing a novel sidegate FET technology. The new FET technology promises to eliminate the Narrow Channel Effect (NCE) which is one of the primary factors limiting the minimum power consumption of integrated circuits. By eliminating the NCE, we will be able to scale the device size dramatically and reduce the power consumption by an order of magnitude. The project will assess the power, speed, circuit design, processing, and manufacturability of the new FET technology for both digital and analog circuit applications. In particular, we will extract device parameters from the new ultra-low power FETs fabricated at UVa, develop device models, incorporate these models into a new SPICE package (AIM-Spice), simulate different logic families including DCFL and SCFL, and compare the predicted performance with the standard DCFL and SCFL logic. We will also analyze the gate current leakage and subthreshold slope as the primary factors limiting the noise margins at low power supplies, establish the minimum required bias voltage for reliable operation, and analyze the factors determining the threshold voltage changes from device to device as well as other factors which may limit the yield and integration scale.

II. Phase I Final Report

The goals of the Phase I STTR project were to develop 2-D MESFET device models and fabrication technologies and to evaluate the advantages and possible disadvantages of a new low power electronics technology based on the 2-D MESFET. The project had five major tasks. These were 1) 2-D MESFET (discrete) device fabrication, 2) detailed device evaluation and optimization for next iteration of device design and fabrication, 3) parameter extraction to generate and refine AIM-SPICE 2-D MESFET models, 4) 2-D MESFET DCFL (direct-coupled FET logic) and SCFL (source-coupled FET logic) circuit simulations using AIM-SPICE and comparison with conventional circuits, and 5) analysis of manufacturability and technology insertion issues. This report summarizes the progress in each task area during the Phase I period 20 OCT 94 - 19 MAY 95.

Task 1: Device Fabrication

A major issue concerning the commercial viability of a low power 2-D MESFET technology is whether 2-D MESFET circuits can be manufactured with high yield and at reasonably low cost. This Phase I project has attempted to address some of the considerations of 2-D MESFET manufacturing (see also summary of Task 5 work). As the 2-D MESFET is a new device [1-3], this project has devoted considerable effort at evaluating and improving the yield of the fabrication process while also generating improved devices for characterization purposes. At the start of this project, the fabrication process was immature and the overall yield was poor, due primarily to an unrefined gate level process. During this project, a gate level dry etch process was developed and implemented into the 2-D MESFET fabrication and at least five wafers were successfully fabricated using the new gate etch process. A sketch and a scanning electron micrograph of a 2-D MESFET fabricated using the new gate processing are shown in Fig. 1. The channel dimensions (the 2-d electron gas region between the two opposing gate contacts) are nominally 1.0 x 0.5 micron ($W_0 \times L_g$) while the source/drain spacing L_{DS} is 2.5 micron. This represents a significant improvement in device uniformity and scaling [4], compared with previous devices, and these improvements are largely responsible for the higher performance devices which are now being fabricated (see summary of Task 2 work).

The dry etch process is similar to those used in the semiconductor industry so manufacturability is not an issue. Two aspects of the fabrication posing significant challenges to manufacturing are the gate metallization and the semiconductor structure design, both of which are different from those used in the large scale manufacturing of digital GaAs ICs, for example. For the 2-D MESFET, the gate metallization is achieved by electroplating the Schottky metals onto the edge of the semiconductor in order to obtain the sidewall Schottky contact. This technique has proven highly reliable in the 2-D MESFET fabrication and it should, in principle, be possible to obtain similar yield and uniformity across large IC wafers. A second fabrication issue impacting the yield is the

design of the semiconductor material structure. The 2-D MESFET utilizes structures which are nearly identical to those used for high performance heterostructure field effect transistors (HFETs), giving the 2-D MESFET a speed advantage compared to the conventional GaAs MESFET. While threshold voltage control is a primary factor limiting the manufacturability of HFET ICs, the 2-D MESFET may have an advantage due to use of the side gates. The HFET threshold voltage is highly sensitive to nanometer variations in the gate-channel separation whereas the 2-D MESFET threshold voltage depends on the much larger gate-gate dimension which we believe will be better controlled. Thus, the primary material issue for 2-D MESFET manufacturing is likely to be cost of the wafers, rather than threshold voltage uniformity, and the cost of wafers is decreasing with increasing volume production.

It is helpful to briefly review why the 2-D MESFET benefits from use of the sidegates and a 2-dimensional electron gas structure. The main reason for the excellent device performance is due to the superior Schottky barrier (gate) characteristics of the 3-d metal/ 2-d electron gas (heterodimensional) junction compared to those of the conventional (3d/ 3d) junction. These two junctions are sketched in Fig. 2. [For the Phase I project, the 2-d electron gas structure was based on the pseudomorphic AlGaAs/InGaAs/GaAs material system.] A fundamental difference between the two junctions is the two-dimensional spreading of the electric field in the 3-d/2-d junction versus the one-dimensional spreading in the conventional 3-d/3-d junction. Another difference is the larger depletion depth (for a given applied voltage) of the 2-dimensional electron gas (2-D MESFET) compared to the volume depletion depth (MESFET) or the parallel 2-d gas channel depth (HFET). **The two-dimensional spreading of the electric field (illustrated in Fig. 2) and the larger depletion depth lead to a smaller junction electric field, larger effective barrier height, lower tunneling current, larger built-in voltage, smaller junction capacitance and a larger breakdown voltage** compared with the conventional Schottky diode. Also, due to a highly degenerate 2-d electron gas, the Fermi level lies in the conduction band, as illustrated in Fig. 3. This leads to a smaller built-in voltage variation with temperature than that for moderately high-doped GaAs such as is used in the GaAs MESFET. As a result, **the 2-D MESFET threshold voltage is virtually independent of temperature** over the military temperature range.

In summary, significant progress in the device fabrication was achieved during the Phase I project and the prospect of further improvement is good. Future work will continue to focus on improving uniformity and yield as well as improving discrete device and integrated circuit performance, through refinements in all levels of fabrication.

Task 2: Evaluation, Optimization, Design

During the Phase I project, several batches of 2-D MESFETs were fabricated and characterized. These included both depletion mode (negative threshold voltage) and enhancement mode (positive threshold voltage) devices. Examples of D-mode and E-mode device current-voltage (I_D - V_{DS}) characteristics are shown in Figs. 4 and 5,

respectively. Note that, since the threshold voltage is determined lithographically (by changing W_0), both D-mode and E-mode devices can be fabricated simultaneously without additional levels of processing. The peak current density (370 mA/mm) and extrinsic transconductance (427 mS/mm) of the D-mode devices are comparable to those of state-of-the-art microwave HFET devices at room temperature, even though the channel width is only 1 micron [5]. The D-mode devices appear to be ideally suited for highly efficient, microwave applications as well as very fast, low power digital logic applications. For smaller widths, the depletion depths of the gates rapidly reduces the effective channel width and the peak current density and transconductance values decrease. On the other hand, the threshold voltage becomes positive, the subthreshold slope increases, the saturation voltage decreases and the output conductance decreases, all of which are beneficial for low voltage (0.5-1.0 V), very low power digital applications. The solid lines in Figs. 4 and 5 are the simulations using the 2-D MESFET device model implemented into AIMSPICE (discussed further in next section).

An advantage the 2-D MESFET has over conventional FETs is greater functionality since the 2-D MESFET has two gates. The dual-gate behavior of a nominally 0.5 x 0.5 micron 2-D MESFET is shown in Fig. 6. Two families of I_D - V_G curves are shown for different voltages on the second gate. The two sets of curves indicate the excellent electrical symmetry when the gates are interchanged. This characteristic is very exciting and opens up many possibilities for level shifting, active loading, electronic tuning of threshold voltage and, of course, 2-input logic elements (see 2-transistor NOR simulations in next section).

As mentioned in the last section, the 2-d electron gas is highly degenerate so that the Fermi level should be only weakly dependent on temperature. As a result, the built-in voltage and the threshold voltage should also be nearly independent of temperature. To test this, we measured I_D - V_{DS} characteristics at different temperatures from room temperature to 150^{o} C. The results, shown in Fig. 7, illustrate the temperature independence of the threshold voltage (here, V_T = -0.6 V) compared to typical GaAs MESFET variation of order 100-150 mV [6]. [The temperature dependence at high gate bias is similar to that observed in conventional Schottky diodes and is due to the temperature dependence of the knee voltage.] The temperature *independence* of the threshold voltage is very significant and should lead to a higher operating temperature range, higher integration densities and simplified circuit design.

Finally, the issue of high series resistance should be addressed. The series resistance of the 2-D MESFET is primarily due to resistance in the 2-d electron gas between the channel and the ohmic contacts and, to a lesser extent, to ohmic contact resistance. The 2-d electron gas resistance is of order 500 Ω/square at room temperature in the current devices and the resistance is higher in the narrower devices. While we expect to reduce the series resistance by reducing the source-drain spacing and possibly through use of ion-implantation, the resistance appears not to affect the device performance at the low current levels used in the circuit measurements. We even simulated 2-D MESFET circuits with zero series resistance and observed a slight trade-off between power and speed (slightly

faster but slightly higher power consumption due to higher current level in the $R_S = 0$ devices). While the high series resistance may be a consideration for microwave applications (i.e. impedance matching), the series resistance should not be a significant issue for digital applications.

Task 3: 2-D MESFET AIM-SPICE Modeling

We have developed a 2-D MESFET model for both the current-voltage and the capacitance-voltage characteristics and both models give excellent agreement with the measured data. The data in Figure 5 include simulated characteristics represented by solid curves. The models are based on the HFET models described in Semiconductor Device Modeling For VLSI by Shur et al [7] but modified to describe the operation of the lateral gates of the 2-D MESFET. These models are implemented into AIM-SPICE and are continuously refined as our understanding of the device progresses. An important feature of the 2-D MESFET current-voltage model is that it describes both the below and above threshold regions of operation with a single analytical expression. This is especially important for circuit simulations where continuous solutions (and their derivatives) lead to better speed and convergence properties compared to other approaches. The capacitance-voltage model also gives excellent agreement with the capacitance extracted from the measured conductance versus voltage characteristic. The models are described in detail in an upcoming publication [5].

We also developed a model which describes the operation of the dual-gated device. In Fig. 8, we compare the measured dual-gate characteristic with the simulated characteristic and an excellent agreement is achieved (the characteristics of the second gate are symmetric, as was shown in Fig. 6, and are therefore omitted for clarity). Having developed accurate 2-D MESFET device models and verified them with measured data, we are able to predict the performance of 2-D MESFET circuits such as the simple DCFL inverter and the ring oscillator. The results of these simulations are discussed next.

Task 4: 2-D MESFET DCFL and SCFL Circuit Simulation

The I-V and C-V AIMSPICE models are being used to design low power DCFL enhancement-depletion logic elements including the basic inverter and variations of a new two-input logic gate, both shown in Fig. 9. For example, the measured and simulated DCFL inverter transfer characteristics using an E/D 2-D MESFET pair are shown in Fig. 10 at supply voltages in the range $0\ V < V_{DD} < 1.0\ V$. The result for $V_{DD} = 0.8$ V is shown in Fig. 11 where the noise margin is found to be 0.26 V which is excellent for such a low voltage technology. By integrating several inverters in series, we have simulated the ring oscillator performance in order to evaluate the potential for future high speed, low power applications. The transient response simulation of a 3-stage 2-D MESFET ring oscillator yielded a total delay of 52 ps (17 ps/stage) at $V_{DD} = 0.8V$ and 48 ps (16 ps/stage) at $V_{DD} = 1.6V$. The results include a delay of 8.7 ps and power of 9.25 uW per gate at $V_{DD} = 0.8V$ or

a power-delay product of less than 0.1 fJ. This result, which is plotted in Fig. 12, represents a very substantial reduction in the power-delay product compared to the state-of-the-art in competing transistor technologies [4]. The main reason for such a reduction in the power-delay product are the elimination of the narrow channel effect (thereby allowing much narrower, lower current devices) and the use of the heterodimensional 3-d/ 2-d Schottky contact which has lower capacitance than the equivalent parallel plate device.

Source-Coupled FET Logic (SCFL) is commonly used for differential amplifiers and other circuits in which an algebraic operation is performed on two or more inputs. Since SCFL utilizes similar gates as are used in DCFL, SCFL should have similar benefits to 2-D MESFET DCFL circuits, including higher speed and lower power operation, greater functionality (using 2-input 2-D MESFET gates) and compatibility with microwave HFET circuits. Our future work will evaluate the design rules and energy efficient operation of 2-D MESFET SCFL circuits using fewer gates and lower supply voltages.

Finally, we simulated a NOR gate using the 2-input model and the result is shown in Fig. 13. The curve on the left is obtained when both gates are biased in common and a typical inverter characteristic is observed. When one gate is left in the OFF state and the second gate is biased, a new output characteristic is obtained (curve on right). The outputs of the 2-input gate are all low except for the case when both inputs are low, thus the gate is a NOR gate. By increasing the threshold voltage further, a NAND gate should be possible. So in addition to operating at a very low power-delay product, 2-D MESFET allows greater functionality using fewer gates -just two transistors for NAND and NOR functions compared with 4 transistors for other digital technologies.

Task 5: Manufacturability and Technology Insertion Issues

This section summarizes the advantages and potential disadvantages of the low power 2-D MESFET technology for digital electronics, including problems which may arise as the integration scale increases. Among the advantages of the 2-D MESFET technology, three appear most significant. First, the 2-D MESFET appears to be a truly low power technology capable of operating at high speed. The Phase I project clearly demonstrated the low power characteristics and the high speed characteristics are inferred from the measured and simulated data. The Phase II research should fabricate and evaluate the ring oscillator circuit to conclusively validate the large reduction in the power-delay product which has been projected in Phase I research. The second significant advantage of the 2-D MESFET is the possibility to reduce the number of transistors for many logic functions by as much as a factor of two, through employing both gates in a 2-input configuration. The Phase I research demonstrated the NOR function using only two transistors. The Phase II research should further investigate the increased functionality of the 2-D MESFET and should demonstrate circuits in which both low power operation and reduced transistor

counts are realized. The third significant advantage of the 2-D MESFET technology is that it is compatible with microwave HFET technology since the two technologies utilize similar structures. The Phase II research should investigate the integration of high speed, low power 2-D MESFET circuits with microwave HFET circuits for digital/analog electronics applications. A fourth advantage of the 2-D MESFET is its smaller temperature dependence of the *I-V* characteristics, particularly the threshold and saturation voltages, over the range 25-150^{0}C where reliability of integrated circuits for military and civilian applications is a critical issue.

The possible disadvantages of the 2-D MESFET technology concern the manufacturability of large scale 2-D MESFET ICs. As was discussed earlier in the *Fabrication* section, the primary differences between the 2-D MESFET fabrication process and that of the GaAs MESFET are the gate metallization and the semiconductor structure. The 2-D MESFET gate is presently formed by electroplating the Schottky metal onto the sidewall of the channel semiconductor. Although electroplating is used in the semiconductor industry, it is usually reserved for large features such as interconnects. In principle, however, we see no reason whythe electroplate technique cannot be used for submicron gate formation on much larger wafers where the uniformity and reliability should only improve. Electroplating has an additional advantage in that there is no waste of metal as there is in conventional deposition techniques. The cost issue of epitaxial growth of heterostructures versus ion implantation of blank GaAs substrates is likely to remain. On the other hand, the demand for higher performance ICs for wireless applications should help drive down the cost of epitaxial wafers in the future.

In spite of our optimism regarding the manufacturability of 2-D MESFET ICs, we are also exploring alternative approaches to realize the benefits of the 2-D MESFET using completely conventional manufacturing techniques. For example, we have begun a parallel effort to evaluate the performance of the 2-D MESFET using conventional ion-implanted GaAs wafers from Vitesse Semiconductor Corporation. The goal of this parallel effort is two-fold: to begin cooperative research with a premier US digital GaAs IC manufacturer from whom we can learn more about manufacturing issues and who may assist us in co-developing the low power 2-D MESFET technology, and to evaluate an alternative and possibly more manufacturable approach to develop a low power 2-D MESFET-based IC technology.

In summary, we are quite optimistic about the future of the 2-D MESFET for low power digital electronics applications. We have made considerable progress during the relatively short Phase I period and we are excited to take the research into the next phase of R&D. The 2-D MESFET is clearly a unique device which has already yielded a glimpse into the rich and superior device fundamentals which are only waiting to be utilized in the rapidly expanding market of advanced, high performance electronics products.

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[1] W.C.B. Peatman, H. Park, B. Gelmont, M. Shur, P. Maki, E.R. Brown and M.J. Rooks, "Novel Metal/2-DEG Junction Transistors," *Proc. IEEE/Cornell Conf. Adv. Conc. in High Speed Semic. Dev. Ckts.*, Ithaca, NY, pp. 314-319, August 1993.

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[5] W.C.B. Peatman, M. Hurt, H. Park, T. Ytterdal, R. Tsai and M. Shur, "Narrow Channel 2-D MESFET for Low Power Electronics," Accepted for publication in *IEEE Trans. on Electron Devices*.

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[7] K. Lee, M. Shur, T.A. Fjeldly, and T. Ytterdal, Semiconductor Device Modeling for VLSI, Prentice Hall, New Jersey, 1993.

IV. Figures

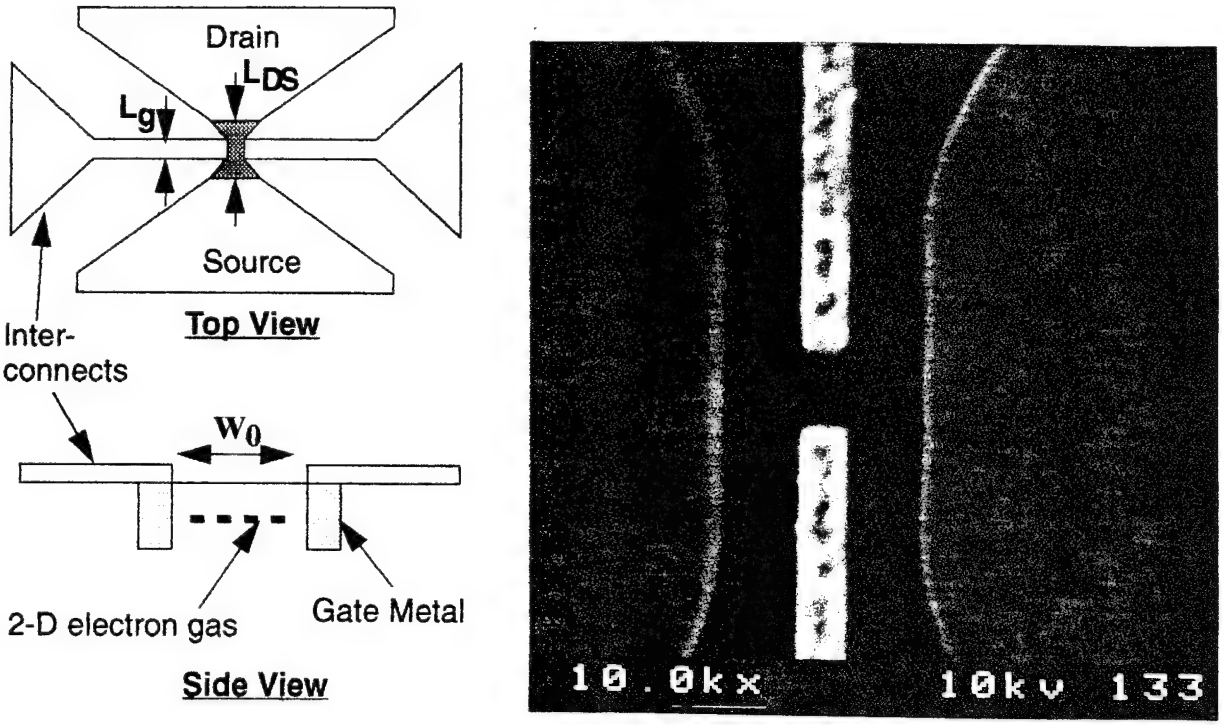

Fig. 1.Sketch (left) and scanning electron micrograph (right) of the 2-D MESFET.

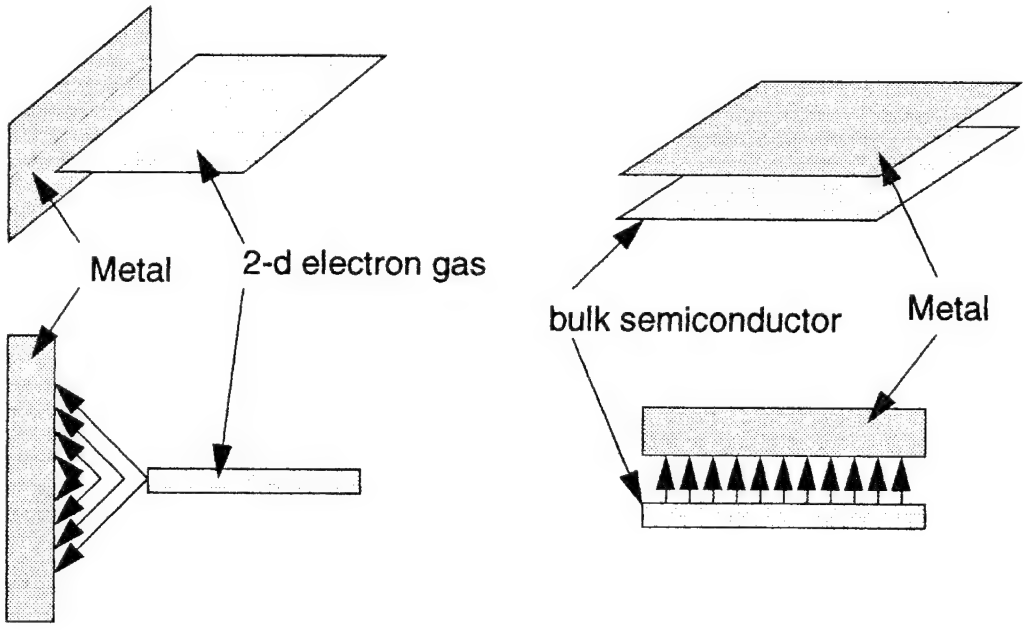

Fig. 2. Perspective and cross-sectional sketches of 3-d/2-d (left) and conventional3-d/3-d (right) Schottky contacts. The electric field spreading in 2-dimensions and larger depletion depth in 3-d/2-d junction leads to higher breakdown voltage and smaller junction capacitance in 2-D MESFET.

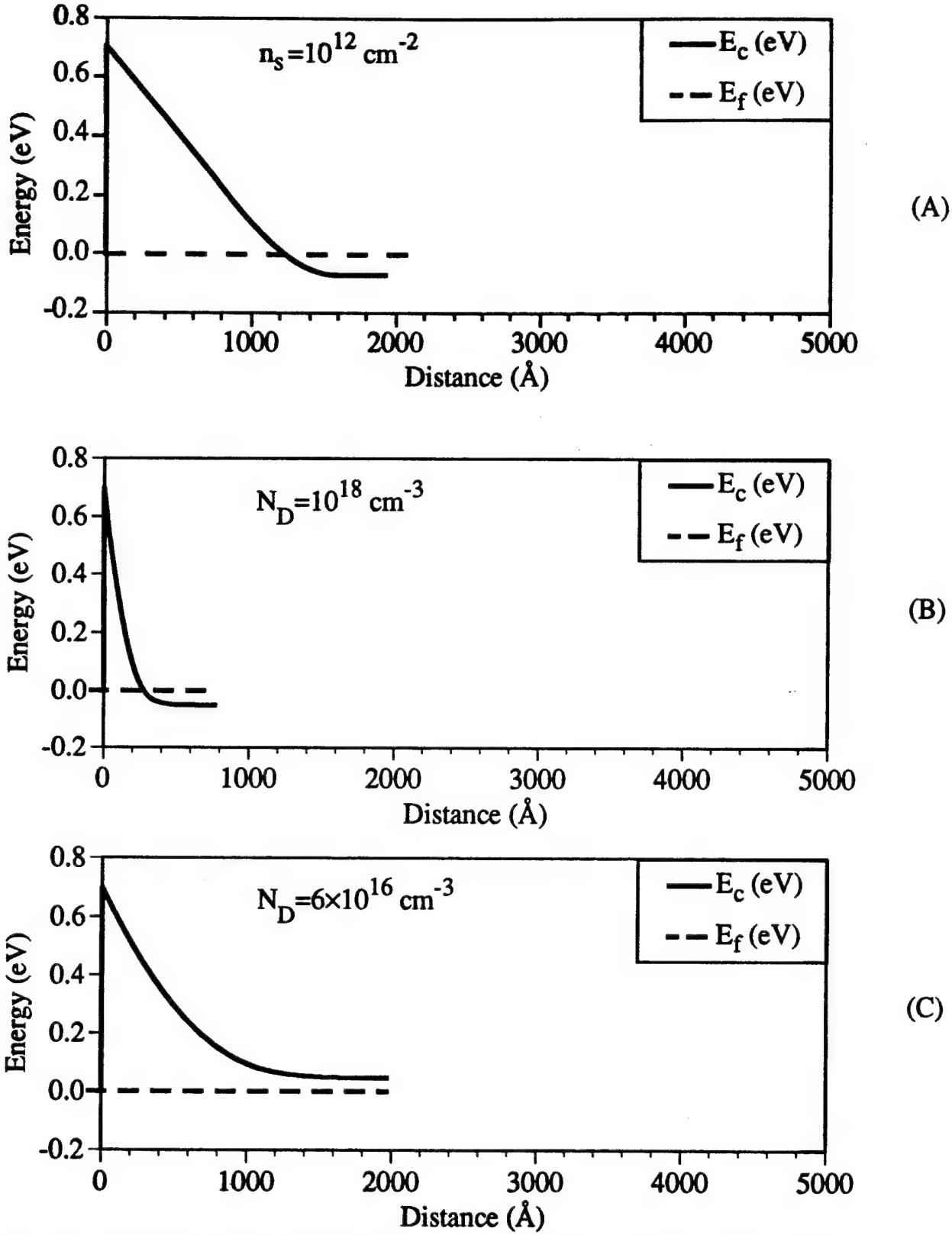

Fig. 3. Comparison of (A) 3-d/2-d Schottky barrier ($n_s = 1 \times 10^{12}$ cm^{-2}) with those of conventional Schottky diodes having: (B) equivalent volume doping ($N_D = 1 \times 10^{18}$cm^{-3}) but only 25 nm depletion depth, and (C) equivalent depletion depth (125 nm) but much lower doping density of 5×10^{16} cm^{-3}.

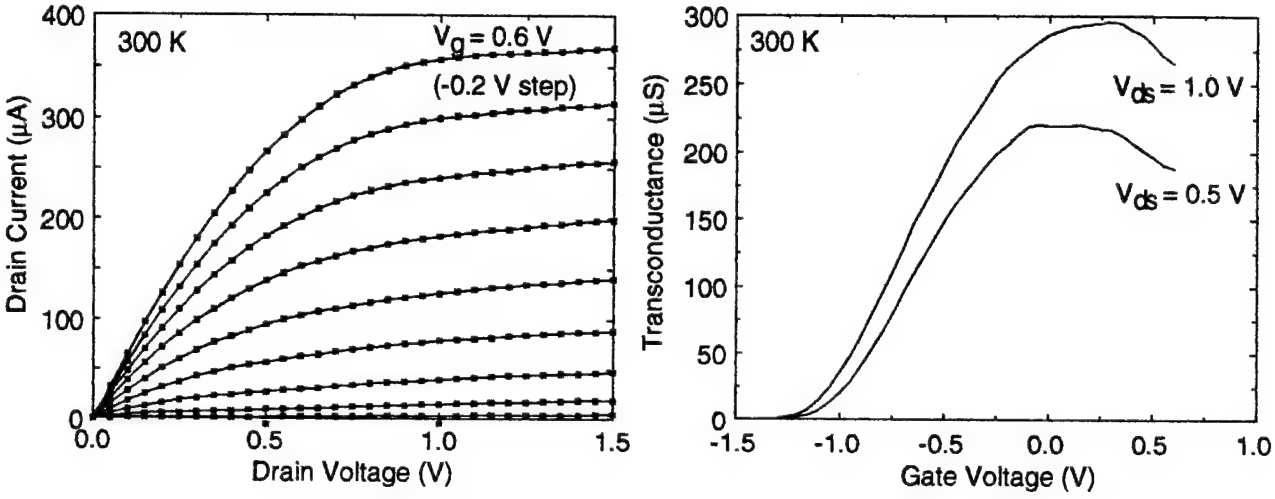

Fig. 4. I_D- V_{DS}(left) and G_m-V_G(right) characteristics of a D-mode 2-D MESFET.

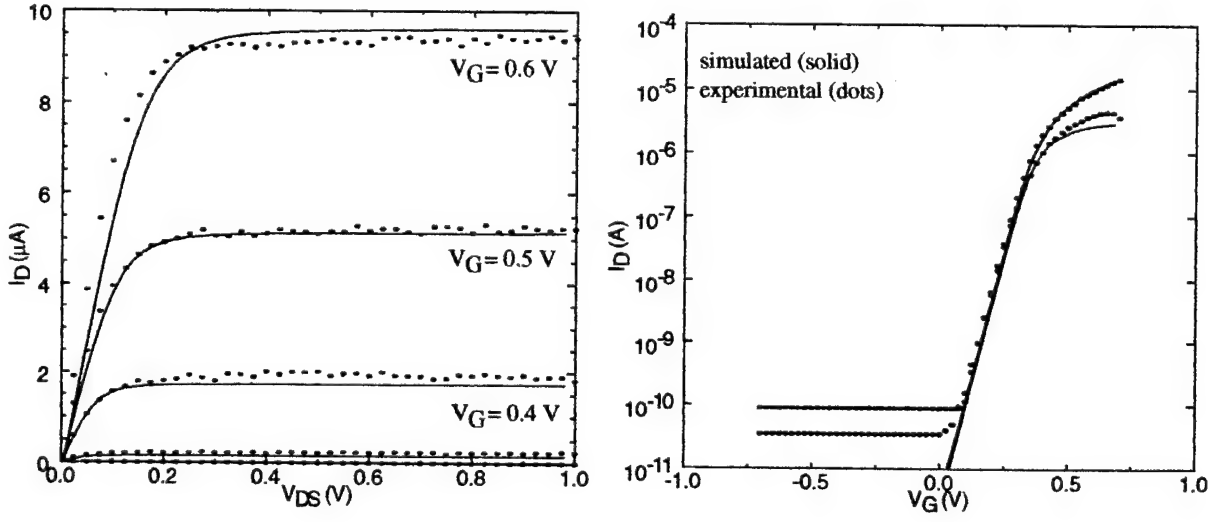

Fig. 5. I_D- V_{DS}(left) and I_D-V_G(right) characteristics of an E-mode 2-D MESFET.

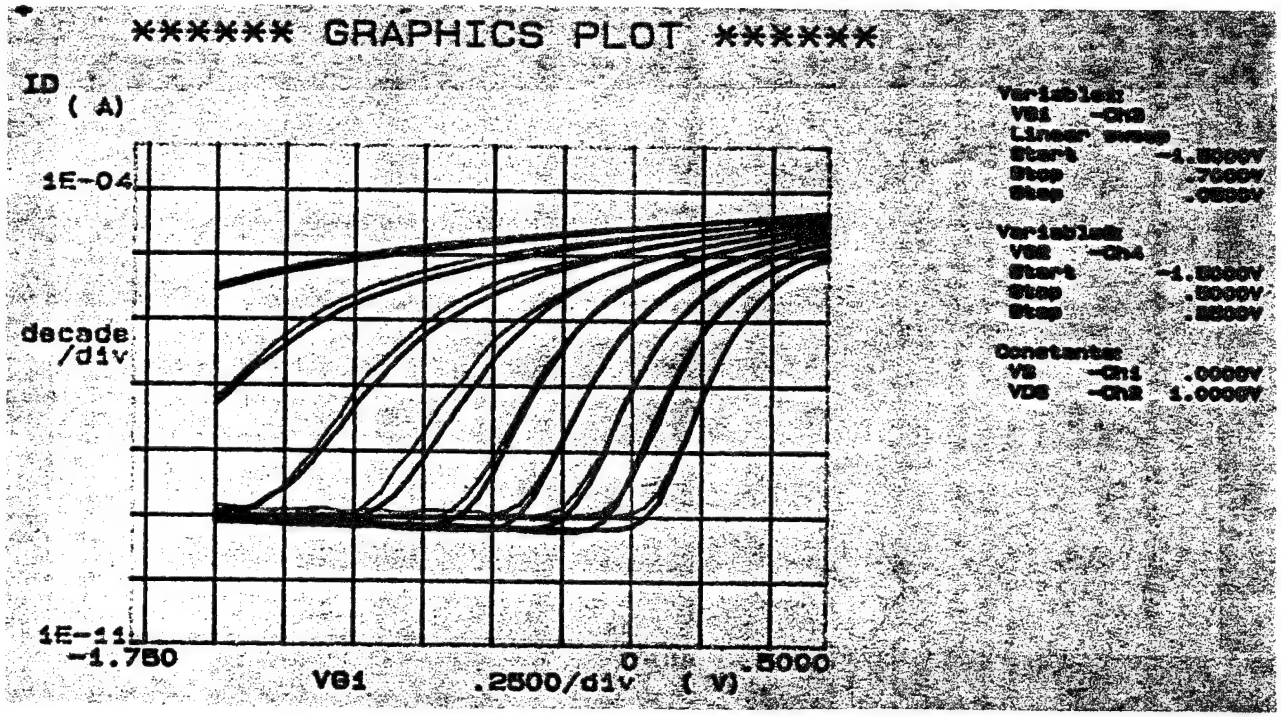

Fig. 6. Families of I_D-V_G characteristics for each gate of the 2-input 2-D MESFET.

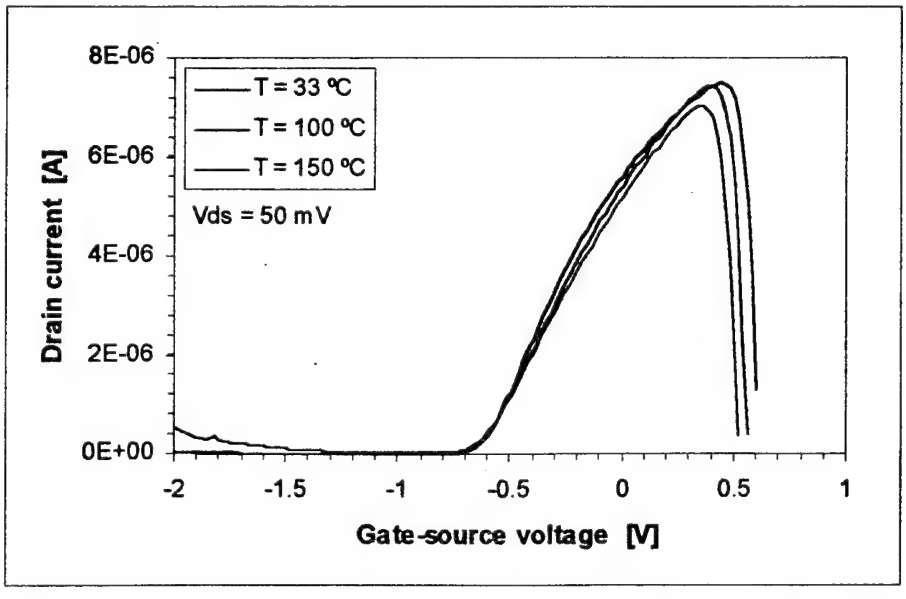

Fig. 7. I_D-V_G (right) characteristics of a D-mode 2-D MESFET at several temperatures.

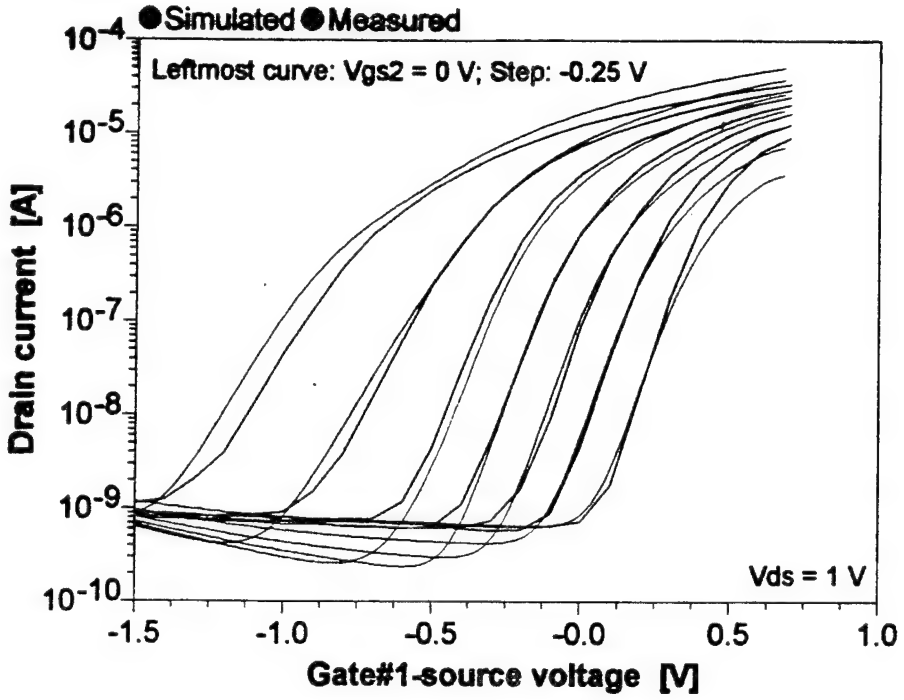

Fig. 8. Measured and simulated I_D-V_G characteristics of the 2-input 2-D MESFET.

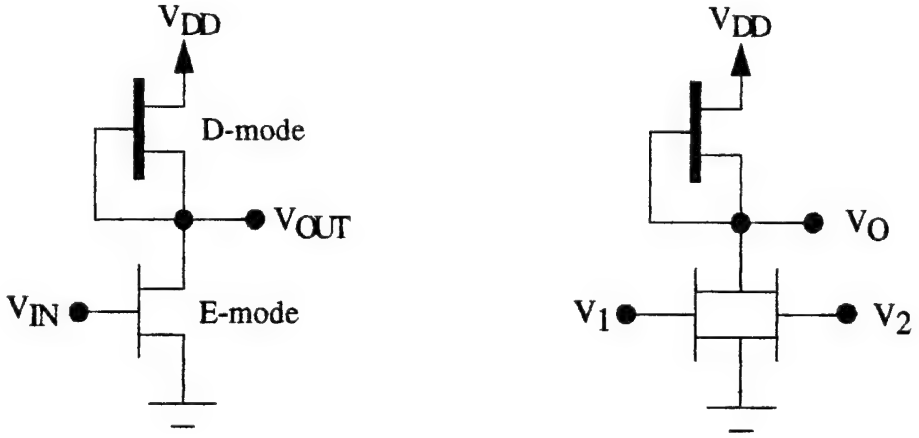

Fig. 9. Wiring diagrams of 2-D MESFET DCFL inverter (left) and NOR gate (right).

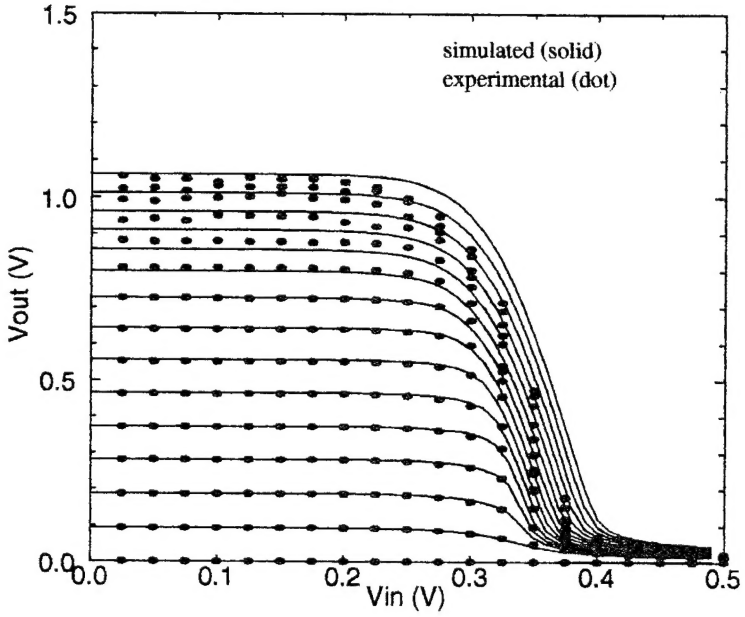

Fig. 10. Measured and simulated 2-D MESFET DCFL inverter transfer characteristics at different supply voltages from $0 < V_{DD} < 1.4$ V.

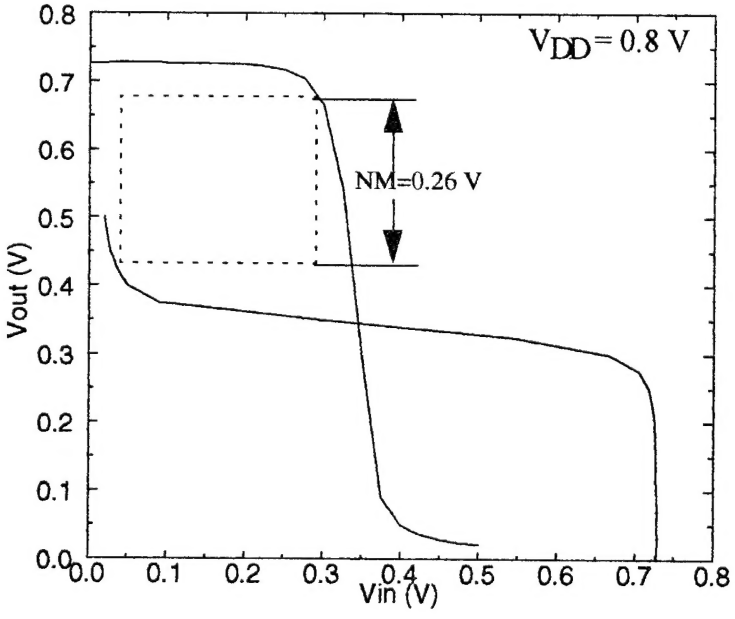

Fig. 11. Measured transfer characteristic and noise margin at V_{DD}= 0.8 V (right).

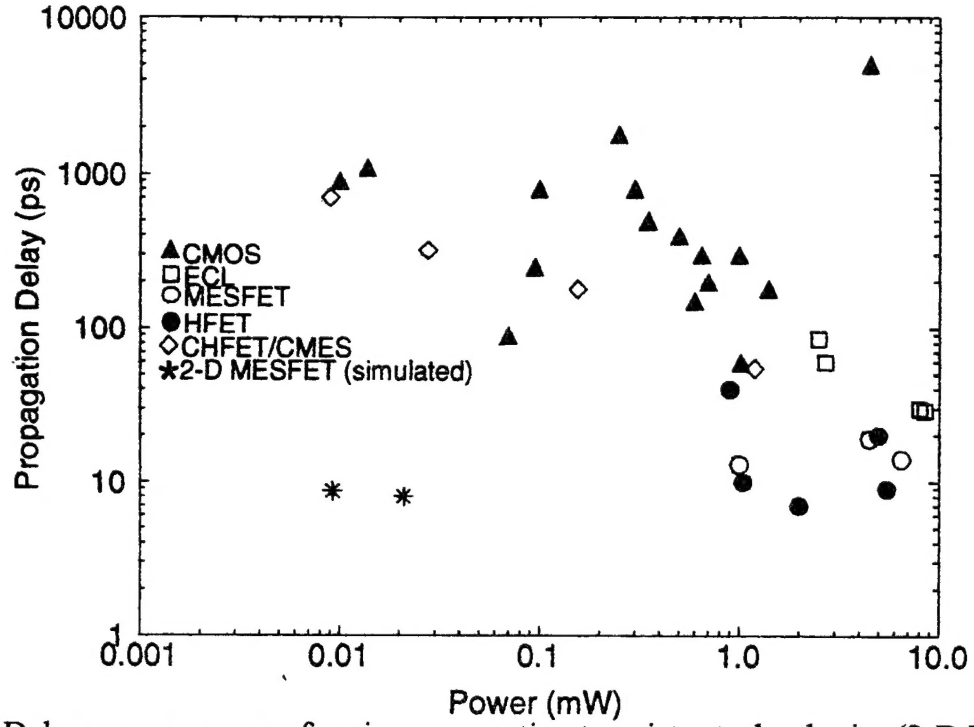

Fig. 12. Delay versus power of various competing transistor technologies (2-D MESFET results are simulated).

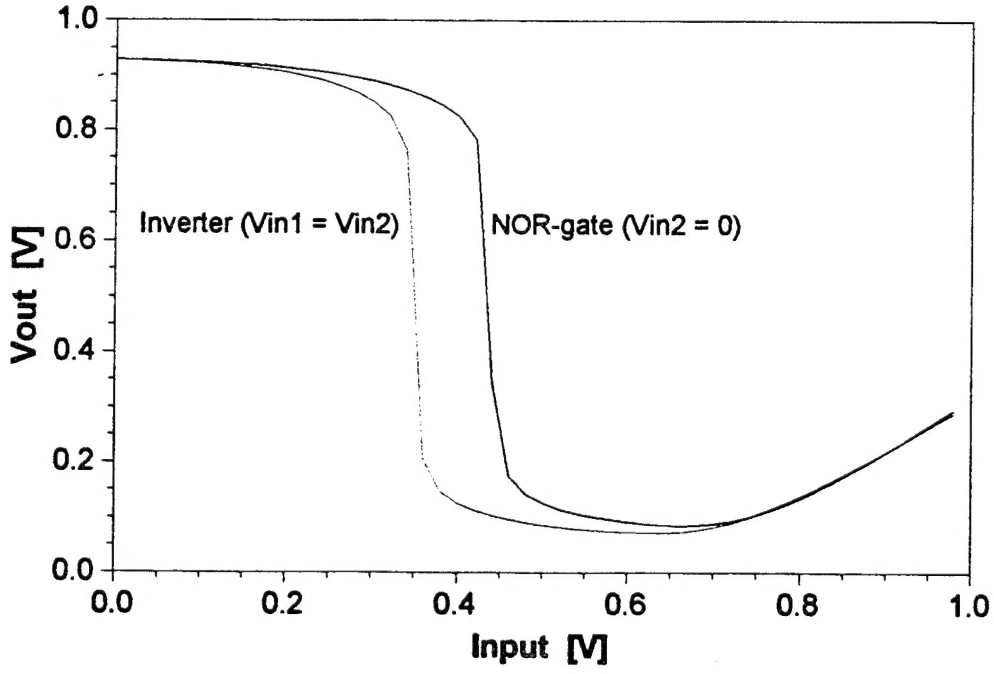

Fig. 13. Simulated transfer characteristics of 2-input gate illustrating NOR function (using only two 2-D MESFETs) at a supply voltage of 1.0 V.

V. Representations and Certifications

DFARS 252.247-7023 TRANSPORTATION OF SUPPLIES BY SEA
No ocean transportation was used in the performance of this contract

DFARS 252.227-7036 CERTIFICATION OF TECHNICAL DATA CONFORMITY
The Contractor, Advanced Device Technologies, Inc., hereby certifies that, to the best of its knowledge and belief, the technical data delivered herewith under Contract No. N00014-94-C-0260 is complete, accurate, and complies with all requirements of the contract.
Date 5/15/95
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